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Performance Enhancement of a Novel Interleaved Boost Converter by Using a Soft-Switching Technique

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ABSTRACT
In this paper a novel Interleaved Boost Converter (IBC) with soft-switching techniques is proposed. Through the zero-voltage switching (ZVS) and zero-current switching (ZCS) reduces the current stress of the main circuit components, in addition to this it can also reduces the ripple of the input current and output voltage. In this approach, it can be faster switching, reduce the size and cost with suitable impedance matching is achieved with reduction in auxiliary circuit reactance that has contributed much increase in the overall performance. Coupled inductor in the boosting stage helps higher current sharing between the switches. The overall ripple and Total harmonics distortions are reduced in this technique without sacrificing the performance and efficiency of the converter. The driving circuit can automatically detect operational conditions depending on the situation of the duty cycle whether the driving signals of the main switches are more than 50% or not and get the driving signal of the auxiliary switch. Auxiliary circuit acts as support circuit to both main switches(two conditions) and reduce the total losses and improve efficiency& power factor for large loads. The operational principle, theoretical analysis, and design method of the proposed converter are presented. The entire proposed system will be tested using MATLAB/SIMULINK and the simulation results are also presented.
Keywords: Interleaved Boost Converter(IBC), Zero-Voltage Switching (ZVS) & Zero-Current Switching (ZCS)

I. INTRODUCTION

A basic boost converter converts a DC voltage to a higher DC voltage. Interleaving adds additional benefits such as reduced ripple currents in both the input and output circuits. Higher efficiency is realized by splitting the output current into two paths, substantially reducing losses and inductor AC losses

In the field of power electronics, application of interleaving technique can be traced back to very early days, especially in high power applications. In high power applications, the voltage and current stress can easily go beyond the range that one power device can handle. Multiple power devices connected in parallel and/or series could be one solution. However, voltage sharing and/or current sharing are still the concerns. Instead of paralleling power devices, paralleling power converters is another solution which could be more beneficial. Benefits like harmonic cancellation, better efficiency, better thermal performance, and high power density.

An interleaved boost converter usually combines more than two conventional topologies, and the current in the element of the interleaved boost converter is half of the conventional topology in the same power condition. The single boost converter can use the zero-voltage switching (ZVS) and/or zero-current switching (ZCS) to reduce the switching loss of the high-frequency switching. However, they are considered for the single topology.

The major challenge of designing a boost converter for high power application is how to handle the high current at the input and high voltage at the output . An interleaved boost dc-dc converter is a suitable candidate for current sharing and stepping up the voltage on high power application. In the interleaved boost converter topology, one important operating parameter is called the duty cycle D.For the boost converter, the ideal duty cycle is the ratio of voltage output and input difference with output voltage.

The PWM converters, the resonant converters are widely employed for high voltage applications because they can easily achieve ZVS or ZCS soft-switching operation during the whole switching transition. However, the series resonant converter has the poor voltage regulation at very light load conditions. The parallel resonant converter is hard to regulate the output voltage at short-circuit conditions. The LCC (one resonant inductor, one

parallel capacitor and one series capacitor) resonant converter and the LLC (one resonant inductor, one magnetizing inductor and one series capacitor) resonant converter have good voltage regulation at light-load and short-circuit conditions. Also, the output diode reverse-recovery problem is alleviated because of its natural commutation of the rectifier current. However, the current through the series capacitor C_r is very large, which needs more bulky capacitors in parallel to reduce the equivalent series resistance (ESR). Meanwhile, the conduction losses are greater than the pulse width modulated (PWM) converters because of its resonant operation mode.

In high-power applications, interleaving of two boost converters is very often employed to improve performance and reduce size of the PFC front end. Namely, because interleaving effectively doubles the switching frequency and also partially cancels the input and output ripples, the size of the energy storage inductors and differential-mode electromagnetic interference (EMI) filter in interleaved implementations can be reduced.

A new active soft switching circuit based on interleaving two boost converters and adding two simple auxiliary commutation circuits is proposed in this paper. Compared to the conventional interleaved boost converters, the main switches are ZCS at turn-on transition and ZVS at turn-off transition. The added auxiliary switches do not cause extra voltages on the main switches and the auxiliary switches are zero-voltage transmission (ZVT) during the whole switching transition. Compared to the previous published soft switching interleaved boost converters, no extra inductor is needed in the auxiliary unit, so the auxiliary unit is simple.

Several soft-switching techniques, gaining the features of zero-voltage switching (ZVS) or zero-current switching (ZCS) for dc/dc converters, have been proposed to substantially reduce switching losses, and hence, attain high efficiency at increased frequencies. The main problem with these kinds of converters is that the voltage stresses on the power switches are too high in the resonant converters, especially for the high-input dc-voltage applications

Converters with interleaved operation are fascinating techniques nowadays. Interleaved boost converters are applied as power-factor-correction front ends. An interleaved converter with a coupled winding is proposed to a provide a lossless clamp. Additional active switches are also appended to provide soft-switching characteristics .These converters are able to provide higher output power and lower output ripple

In ZVT and ZCT converters, an auxiliary circuit containing resonant elements and an auxiliary switch is used that provide soft switching at switching instances and is usually incapable of transferring energy from an input source to output. In some of these converters or some members of converter family, the auxiliary circuit can boost the effective duty cycle, but the amount of energy that is transferred through the auxiliary circuit cannot be controlled once the converter is designed. In the ZVT converter family introduced in, the output current can be shared between main and auxiliary switches even though the authors did not have the intention of current sharing for these converters. In ZCT converters introduced in, the output current is shared between the switches; however, the switches do not turn off under soft-switching condition.

The main intension of the paper is to develop the zero voltage switching and zero current switching actions in boost converter by using interleaved approach to mainly reduce the sudden voltage and current changes(on & off).Auxiliary circuits acts as support circuit to both main switches (two conditions) and reduce the total losses and improve efficiency& power factor for large loads. The voltage stresses of the main switches and auxiliary switch are equal to the output voltage and the duty cycle of the proposed topology can be increased to more than 50%. The proposed converter is the parallel of two boost converters and their driving signals stagger 180◦ and this makes the operation assumed symmetrical. Moreover, by establishing the common soft-switching module, the soft-switching interleaved converter can further reduce the size and cost.

II. ANALYSIS OF OPERATION

Fig: 1 shows the proposed circuit. It uses the interleaved boost topology and applies the common soft-switching circuit. The resonant circuit consists of the resonant inductor L_r , resonant capacitor C_r , parasitic capacitors C_{sa} and C_{sb}, and auxiliary switch s_r to become a resonant way to reach ZVS and ZCS functions. Fig: 2 shows the two operating modes of this circuit, depending on whether the duty cycle of the main switch is more than 50% or not.

Operational Analysis of D <50% Mode

The operating principle of the proposed topology is described in this section. There are 24 operational modes in the complete cycle. Only the 12 modes related to the main switch *Sa* are analyzed, because the interleaved topology is symmetrical. Fig: 3 shows the related waveforms when the duty cycle of the main switch is less than 50%. There are some assumptions to simplify the circuit analysis.

1) All switches and diodes are assumed ideal.
2) Idealizing the input and output reactance.
3) The two boost inductors are equal.
4) The duty cycles (D1 = D2) for the main switches s_a and s_b.

Mode 1 [$\mathbf{t_0 - t_1}$]: Fig: 4 (a) shows the equivalent circuit. In this mode, the main switches S_a and S_b are turned OFF, the auxiliary switch S_r and the rectifier diodes D_a and D_b are turned ON, and the clamped diode D_r is turned OFF. The voltages across the parasitic capacitors C_{sa} and C_{sb} of the main switches and the resonant capacitor *Cr* are all equal to the output voltage; i.e. $V_{sa} = V_{sb} = V_{sr} = V_0$ in the previous mode.

The resonant inductor current I_r linearly ramps up until it reaches I_{in} at $t = t_1$. When the resonant inductor current I_{Lr} is equal to I_{in}, the mode 1 will end. Then, the rectifier diodes are turned OFF. The interval time t_{01} is

$$t_{01} = L_r . \frac{I_{Lr}}{V_0} \qquad (1)$$

Mode 2 [$\mathbf{t_1 - t_2}$]: In mode 2, the resonant inductor current continues to increase to the peak value, and the main switch voltages V_{Sa} and V_{Sb} decrease to zero, because the resonance occurs among $C_{sa}, C_{sb} C_r$ and L_r. Then, the body diodes D_{sa} (S_a) and D_{sb} (S_b) can be turned ON as shown in Fig: 4(b)

The resonant time t_{12} and resonant inductor current i_{Lr} (t_2) are

$$t_{12} = \frac{\pi}{2\omega_0 0} = \frac{\pi}{2} . \sqrt{L_r . (C_{sa+} C_{sb} + C_r)} \qquad (2)$$

$$I_{Lr} = nI_{in} + \frac{V_0}{Z_0} = I_{in} + \frac{V_0}{\sqrt{\frac{L_r}{(C_{sa} + C_{sb} + C_r)}}} \qquad (3)$$

where

$$\omega_0 = 1/\sqrt{L_r . (C_{sa} + C_{sb} + C_r)}$$

And $Z_0 = \sqrt{L_r/(C_{sa} + C_{sb} + C_r)}$

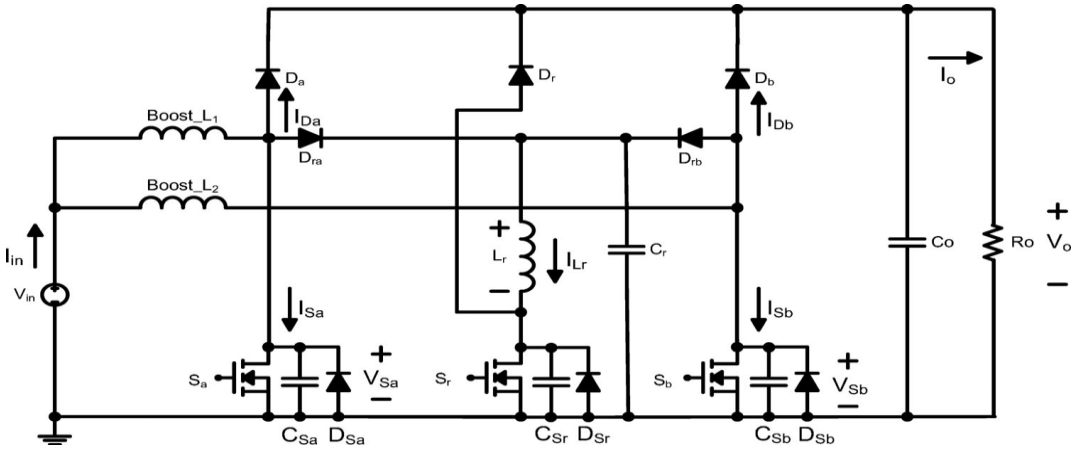


Fig: 1 A novel interleaved boost converter with characteristics of zero-voltage switching and zero-current switching

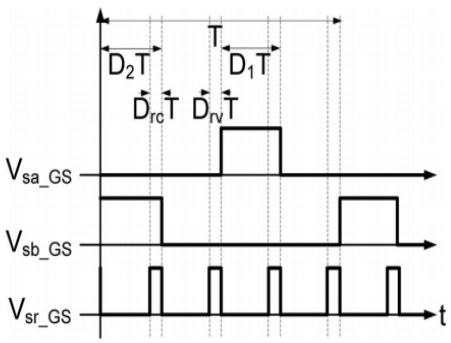


Fig: 2 Switching waveforms of the main switches S_a and S_b

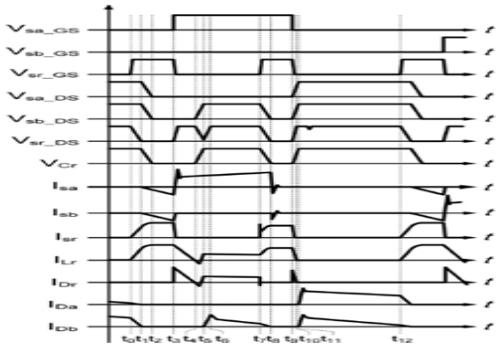


Fig:3 Related waveforms (D < 50%). And auxiliary switch S_r.(a)D < 50% mode

Mode 3 [t_2–t_3]: Fig: 4(c) shows the equivalent circuit of this mode. At the end of mode 2, the main switch voltage V_{Sa} decreases to zero, so the body diode D_{sa} of S_a is turned ON at t_2 . At this time, the main switch can achieve ZVS. The on-time t_{03} of the auxiliary switch Sr needs to be more than t_{01}+t_{12} to achieve the function of ZVS.
The interval time t_{03} is

$$t_{03} \geq t_{01} + t_{12} = L_r.\frac{I_{in}}{V_o} + \frac{\pi}{2}.\sqrt{L_r.(C_{sa}+C_{sb}+C_r} \quad (4)$$

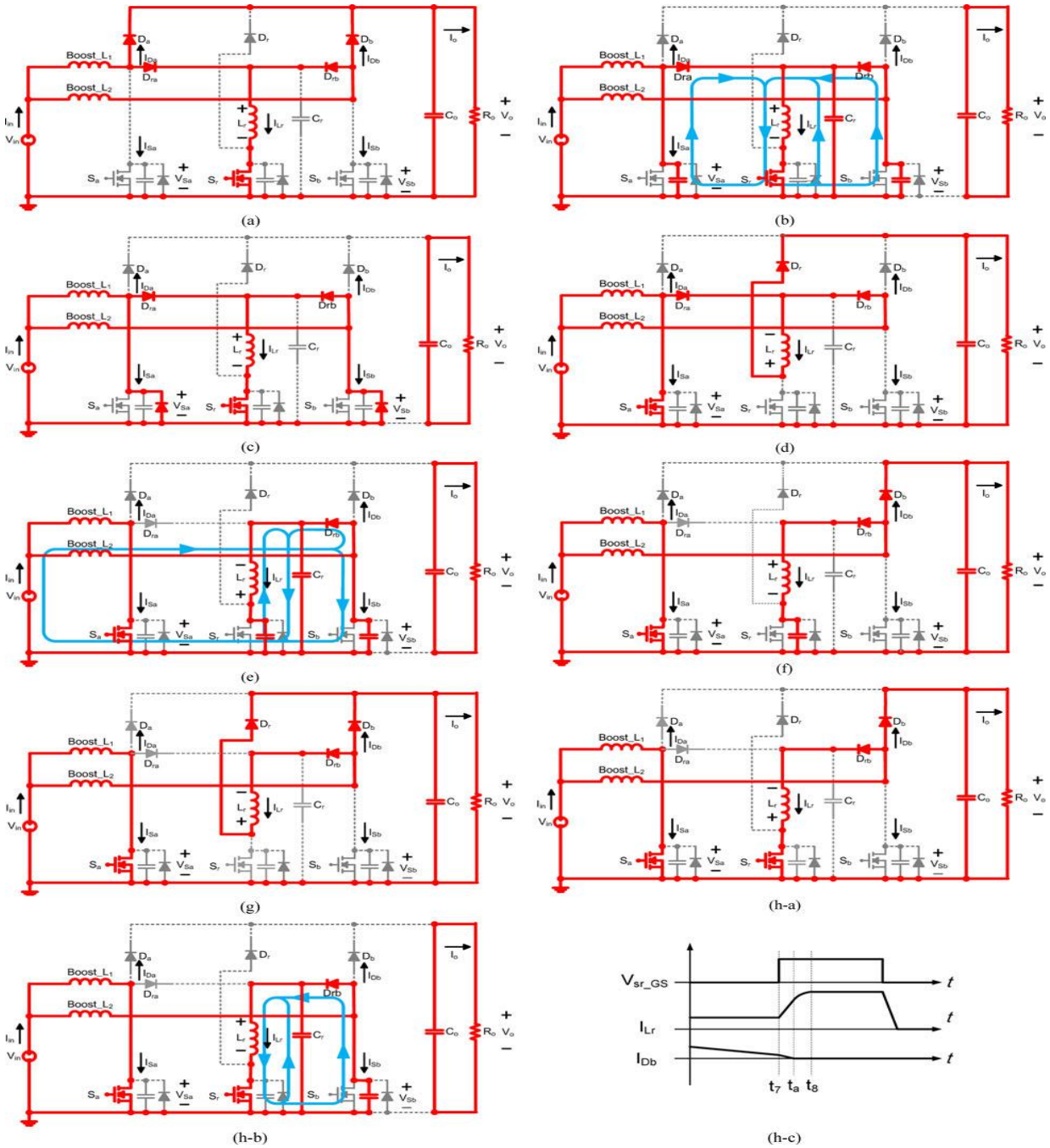


Fig:4 Equivalent circuits of different modes (D < 50%). (a) Mode 1 [t_0 –t_1]. (b) Mode 2 [$t_1 - t_2$]. (c) Mode 3 [$t_2 - t_3$]. (d) Mode 4 [$t_3 - t_4$]. (e) Mode 5 [$t_4 - t_5$].(f) Mode 6 [t_5 –t_6] (g) Mode 7 [t_6 –t_7]. (h-a) Mode 8 [t_7 –t_a]. (h-b) Mode 8 [t_a –t_8]. (h-c) Detailed waveform of the Mode 8.

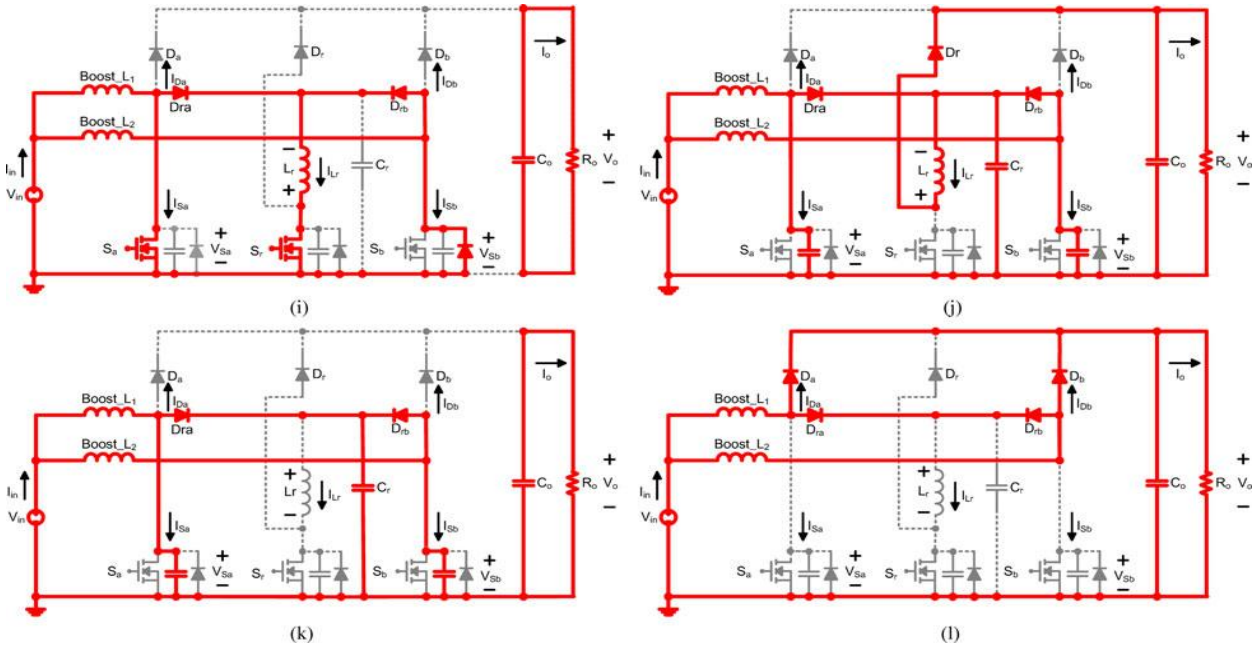


Fig. 4 (Continued.) Equivalent circuits of different modes (D <50%). (i) Mode 9 [t_8–t_9]. (j) Mode 10 [t_9 –t_{10}]. (k) Mode 11 [t_{10} –t_{11}]. (l) Mode 12 [t_{11} –t_{12}].

Mode 4 [$t_3 - t_4$]: Fig: 4 (d) shows the equivalent circuit of this mode. In this mode, the auxiliary switch S_r is turned OFF, and the clamped diode D_r is turned ON. During this interval, the energy stored in the resonant inductor L_r is transferred to the output load.

The resonant inductor current I_{Lr} decreases to zero and the clamped diode D_r is turned OFF at t_4. The energy discharge time of the resonant inductor is

$$t_{34} = \frac{L_r}{V_o}\left(I_{in} + \frac{V_o}{\sqrt{L_r/(C_{sa} + C_{sb} + C_r)}}\right). \qquad (5)$$

Mode 5 [$t_4 - t_5$]: In this mode, the clamped diode D_r is turned OFF. The energy of the boost_L2 is transferred to Cr and C_{sb} and the energy stored in the parasitic capacitor C_{sr} of the auxiliary switch is transferred to the inductor L_r and resonant capacitor C_r at this time. The rectifier diode D_b is turned ON when the voltage across the main switch S_b reaches V_o at t =t_5 .

The resonant inductor current $i_{Lr}(t)$ is

$$i_{Lr}(t) = -V_o\sqrt{\frac{CC_{Sr}}{L_r(C + C_{Sr})}}\,sin\sqrt{\frac{C + C_{Sr}}{L_r CC_{Sr}}}t + \frac{I_{L2}C_{Sr}}{C + C_{Sr}} \times\left(1 - cos\sqrt{\frac{C + C_{Sr}}{L_r CC_{Sr}}}t\right) \qquad (6)$$

The resonant time t_{45} is

$$t_{45} = \pi\sqrt{\frac{L_r CC_{Sr}}{C + C_{Sr}}} \qquad (7)$$

Where,$C = C_{sb} + C_r$

Mode 6 [$t_5 - t_6$]: Fig : 4(f) shows the equivalent circuit. The parasitic capacitor C_{Sr} of the auxiliary switch is linearly charged by I_{L2} −I_o toV_o. Then, the clamped diode D_r is turned ON at t_6.

The interval time t_{56} is

$$t_{56} = \frac{C_{Sr}.V_o}{I_{L2} - I_o}. \qquad (8)$$

Mode 7 [$t_6 - t_7$]: Fig: 4(g) shows the equivalent circuit. In this mode, the clamped diode D_r is turned ON. The energy stored in the resonant inductor L_r is transferred to the output load by the clamped diode D_r.At t_7, the clamped diode D_r is turned OFF because the auxiliary switch S_r is turned ON.

The interval time t_{67} and the resonant inductor current are

$$t_{67} = D_1 T - (D_{rc}T + t_{36}) \qquad (9)$$

$$i_{Lr}(t_7) \approx i_{Lr}(t_6) = I_{L2} - I_o. \qquad (10)$$

Mode 8 $[t_7 - t_8]$: In the interval $[t_7 - t_a]$, the resonant inductor current I_{Lr} increases linearly until it reaches I_{L2} and the rectifier diode current I_{Db} decreases to zero at $t = t_a$, so the rectifier diode D_b is turned OFF. Fig: 4(h-a) shows the equivalent circuit. The interval time t_{7a} is

$$t_{7a} = L_r.\frac{I_o}{V_o}. \quad (11)$$

As for the interval time $[t_a - t_8]$.Fig: 4$[t_a - t_8]$.The resonant inductor current continues to increase to the peak value and the main switch voltage V_{sb} decreases to zero because of the resonance among C_{Sb}, C_r, and L_r. At $t = t_8$, the body diode D_{sb} of S_b is turned ON.

The interval time t_{a8} is

$$t_{a8} = \frac{\pi}{2\omega_1} = \frac{\pi}{2}.\sqrt{L_r(C_{Sb} + C_r)} \quad (12)$$

Then, t_{78} is

$$t_{78} = L_r.\frac{I_o}{V_o} + \frac{\pi}{2}.\sqrt{L_r(C_{Sb} + C_r)}\ . \quad (13)$$

Mode 9 $[t_8 - t_9]$: In this mode, the resonant inductor current I_{Lr} is equivalent to a constant current source.Fig :4(i) shows the equivalent circuit. In order to meet the demand that the main switch Sa is turned OFF under the ZCS condition, $i_{Lr}(t_8) \approx i_{Lr}(t_9)$ must be greater than I_{in}. Then the main switch currents I_{sa} and I_{sb} are less than or equal to zero, so the main switch S_a is turned OFF under the ZCS condition.

The interval time t_{89} is

$$t_{89} = D_1T - t_{38}. \quad (14)$$

And, the zero-current switching conditions are

$$i_{Lr}(t_8) \approx i_{Lr}(t_9) = i_{Lr}(t_a) + \frac{V_o}{\sqrt{L_r/(C_{sb} + C_r)}} \geq I_{in} \quad (15)$$

and the duty time of ZCS is longer than the interval time t_{78} ($D_{rc}T > t_{78}$).

Mode 10 $[t_9 - t_{10}]$: When the main switch S_a and the auxiliary switch S_r are turned OFF, the energy stored in the resonant inductor L_r is transferred to the output load by the clamped diode D_r . When the resonant inductor current I_{Lr} decreases to zero at t_{10}, the clamped diode D_r is turned OFF. Then, the capacitorsC_{sa}, C_{sb}, and C_r are charged by I_{in} as shown in Fig: 4(j).

The interval time t_{9-10} and capacitor voltages of C_{sa}, C_{sb}, and C_r are

$$t_{9-10} = \frac{L_r}{V_o}\left(i_{Lr}(t_a) + \frac{V_o}{Z_1}\right)$$

$$= \frac{L_r}{V_o}\left(i_{Lr}(t_a) + \frac{V_o}{\sqrt{L_r/(C_{sb} + C_r)}}\right) \quad (16)$$

$$V_{Cr}(t_{10}) = V_{Sa}(t_{10}) = V_{Sb}(t_{10})$$

$$= \frac{1}{(C_{sa} + C_{sb} + C_r)}\int_{t_9}^{t_{10}}[I_{in} - i_{Lr}(t)]\,dt. \quad (17)$$

Mode 11 $[t_{10} - t_{11}]$: The capacitors C_{sa}, C_{sb}, and C_r are linearly charged by I_{in} to V_o, and the rectifier diodes D_a and D_b are turned ON at t_{11}. as shown in Fig: 4(k).

This charged time t_{10-11} is

$$t_{10-11} = \frac{(C_{sa} + C_{sb} + C_r).(V_o - V_{Cr}(t_{10}))}{I_{in}} \quad (18)$$

Mode 12 $[t_{11} - t_{12}]$: In this mode, the operation of the interleaved boost topology is identical to that of the conventional boost converter. The ending time t_{12} is equal to the starting time t_0 of another cycle, because the operation of the interleaved topology is symmetrical. As shown in Fig :4(l)

The interval time t_{11-12} is

$$t_{11-12} = \frac{T}{2} - (D_1T + t_{03} + t_{9-11}). \quad (19)$$

Voltage Ratio of D < 50% Mode Fig: 5 shows the equivalent circuits about the operation for the boost inductor Boost_L_1 . The inductor Boost_L_2 has the similar results. So, when the switch is turned ON, the boost inductor current can be derived to be

$$\sum_{Sa=on} \Delta i_{L1} = \frac{V_{in} \times (\Delta t_{bc} + \Delta t_{dc} + \Delta t_{ef} + \Delta t_{fg} + \Delta t_{hi})}{L_1} = \frac{V_{in} \times (D_1 + D_{rc} + 2D_{rv})T}{L_1} \quad (20)$$

And when the switch is turned OFF, the boost inductor current is

$$\sum_{Sa=off} \Delta i_{L1} = \frac{(V_{in} - V_o) \times (\Delta t_{ab} + \Delta t_{cd} + \Delta t_{gh})}{L_1}$$

$$= \frac{(V_{in} - V_o) \times [1 - (D_1 + D_{rc} + 2D_{rv})]T}{L_1}. \quad (21)$$

Then, the voltage conversion ratio can be derived to be

$$\frac{V_o}{V_{in}} = \frac{1}{1 - (D_1 + D_{rc} + 2D_{rv})}. \quad (22)$$

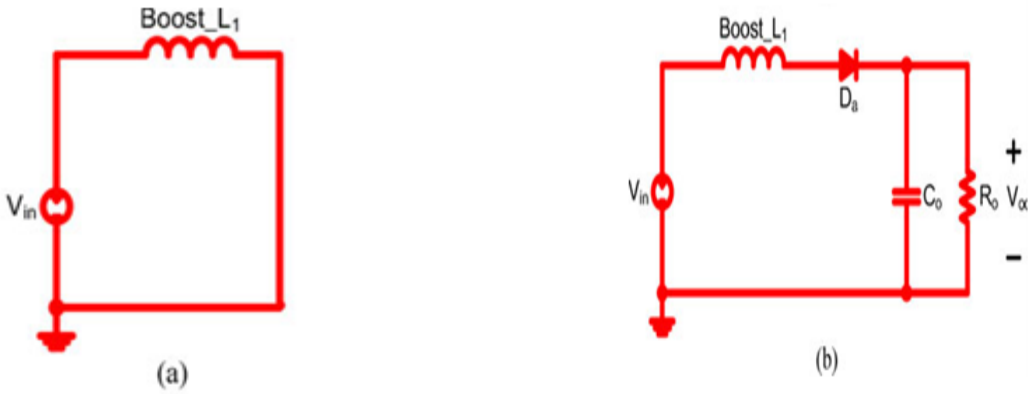


Fig.5 Equivalent circuits for the boost inductor (D < 50%) (a) Boost_L_1 in the stage (b) Boost_L_1 in the stage with output capacitor

III. SIMULATION RESULTS

A .Simulation Circuit From Operational Analysis Of D <50% Mode

Fig: 6 show the simulink model of proposed diagram from D<50% . Fig: 7 show the simulation results. They verify the operation of the proposed circuit. The proposed Interleaved Boost Converter with both ZVS and ZCS characteristics was built.

Fig: 8 show the simulink model of proposed diagram from D>50% .Fig:9 show the simulation results. They verify the operation of the proposed circuit. The proposed Interleaved Boost Converter with both ZVS and ZCS characteristics was built

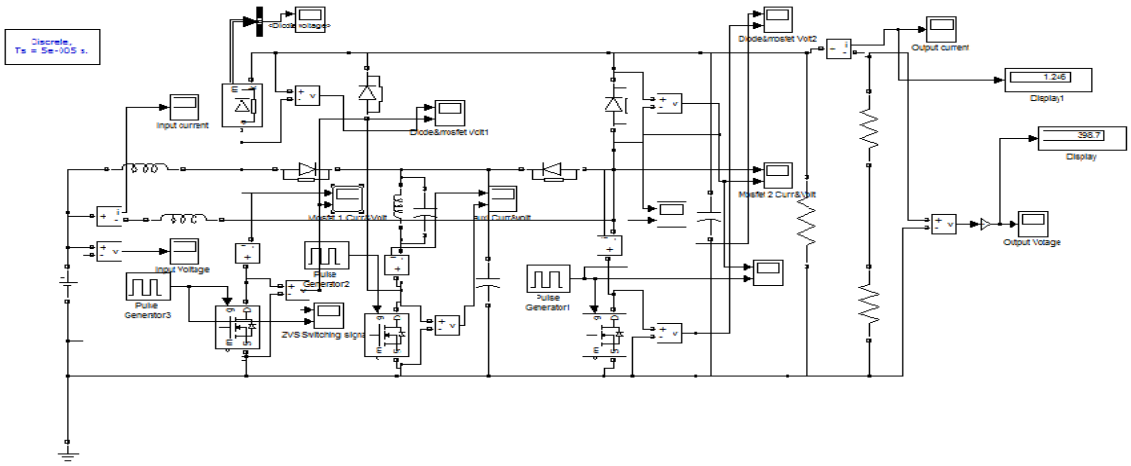
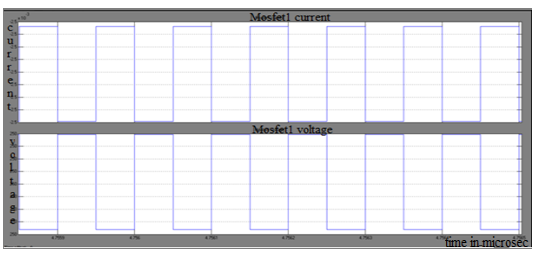
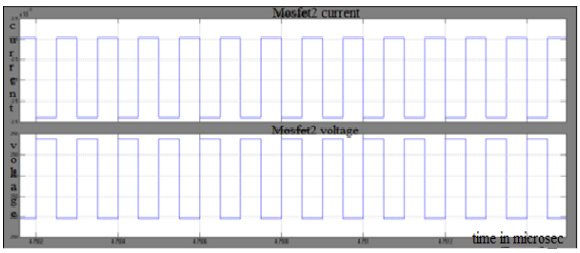


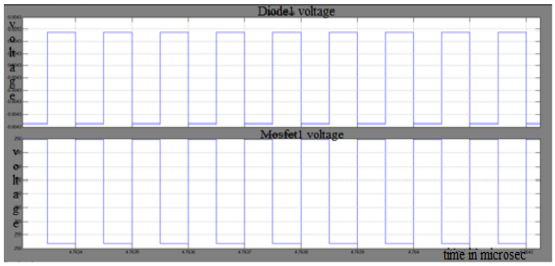
Fig: 6 Simulink Model of Proposed diagram from D<50%



(a)



(b)



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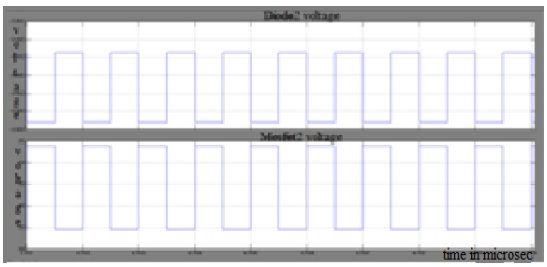
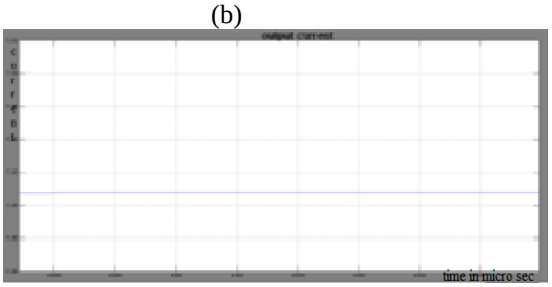
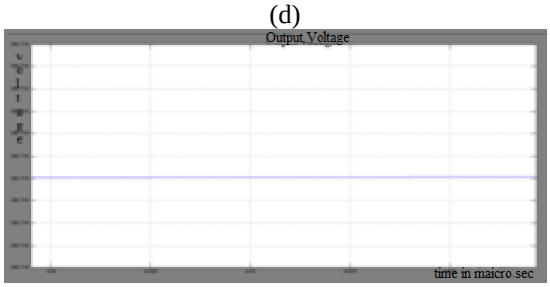


(d)



(e)



(f)

Fig:7 simulation waveforms of the main switches $\mathcal{S}_a$ and $\mathcal{S}_b$ (D<50% and load current 1.5A) (a)Mosfet1 Current & Voltage, (b)Mosfet2 Current & Voltage,(c)Diode1 & Mosfet1 Voltage,(d)Diode2 & Mosfet2 Voltage,(e) Output Current,(f) Output Voltage

B.Simulation Circuit From Operational Analysis Of D >50% Mode

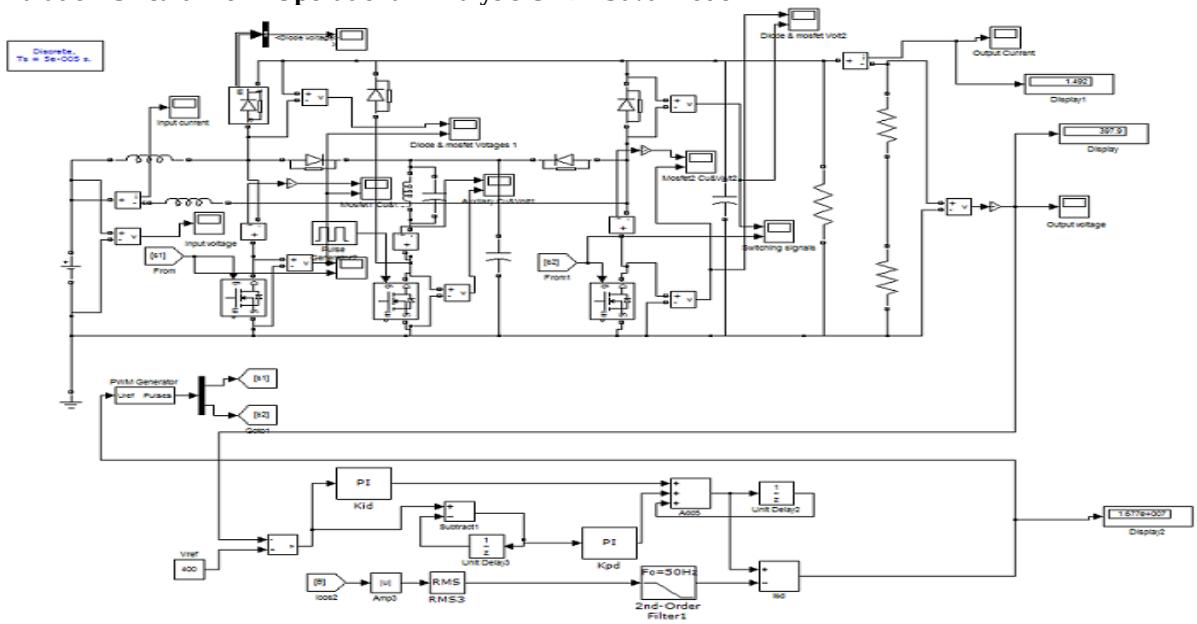
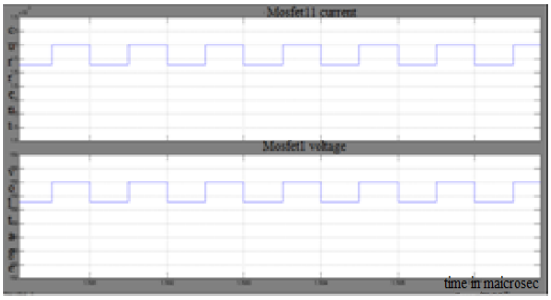
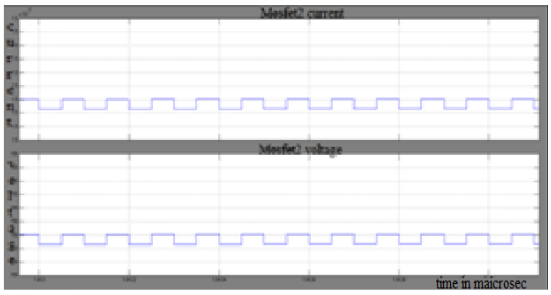


Fig: 8 Simulink Model of Proposed diagram from D>50%



(a)



(b)

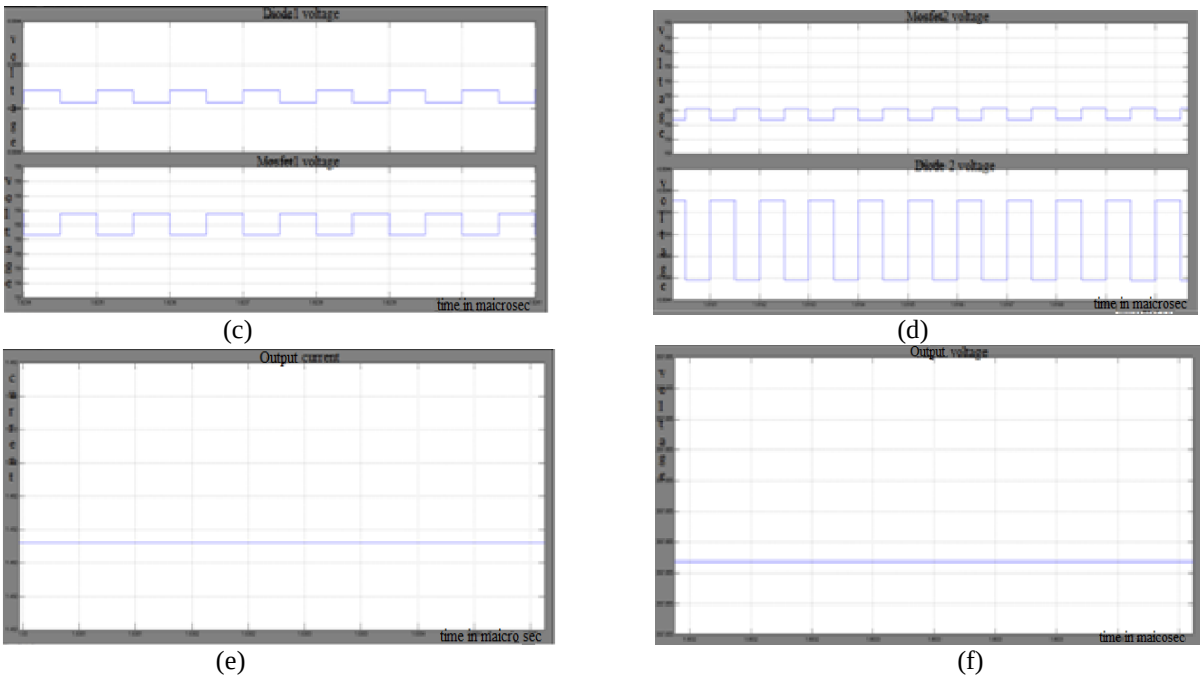


Fig:9 simulation waveforms of the main switches S_a and S_b (D>50% and load current 1.5A) (a) Mosfet1 Current & Voltage , (b) Mosfet2 Current & Voltage , (c) Diode1 & Mosfet1 Voltage, (d) Diode2 & Mosfet2 Voltage, (e) Output Current, (f) Output Voltage

IV. CONCLUSION

High efficiency of step-up DC/DC converters can be achieved by decreasing duty cycle (lower conduction losses) and reducing voltage stress on switches (cheaper and lower RDS−on switches) applying soft switching technique (minimizing switching losses).

The main switches S_a and S_b can achieve both ZVS and ZCS. The voltage stress of all switches is equal to the output voltage. It has the smaller current stress of elements. It uses the resonant inductor L_r , resonant capacitor C_r , parasitic capacitors C_{sa} and C_{sb}, and auxiliary switch S_r to become a common resonant way to reach ZVS and ZCS of the main switches S_a and S_b .The driving circuit can automatically detect whether the driving signals of the main switches are more than 50% or not and get the driving signal of the auxiliary switch. The users can only apply the ZVS or ZCS function just by the adjustment of the driving circuit. The efficiency is 94.6% with output power of 600W and input voltage of 150V and it is 95.5% with output power of 400W and input voltage of 250V

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